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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,426	03/09/2004	Brian Robert Prasky	POU920030068US1	1895

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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04/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,426	PRASKY ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,8-14,19-25,27,28,30,31,34,38-41 and 46-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8-14,19-25,27,28,30,31,34,38-41 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, 8, 9-14, 19-25, 27, 28, 30, 31, 34, 38-41, and 46-50 are pending.

Papers Filed

2. Examiner acknowledges receipt of amendments and remarks filed 16 January 2008.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 16 January 2008 has been entered.

Non-compliant Claim Objections

1. The following claims are still non-compliant: 4, 19, 20, 26, 30, 34, 38, 39, 46.

Examiner urges Applicant to review MEPE 1.121

Claim Objections

3. It appears that Applicant intended to cancel claim 25. They relate to the same basis as cancelled claim 2 and their limitations are included in independent claim 24.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 8-13, 19-28, 30, 31, 34, 38-40, and 46-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al. (U.S. Patent No. 6,425,075) in view of Cummins (U.S. Patent No. 6,263,427).

5. As per claim 1, Stiles teaches a method of operating a computer having a pipelined processor having a branch target buffer (BTB) (Fig. 2 cache 155 and 152) comprising creating a recent entry queue (Fig. 2 cache 152) said recent entry queue comprising a set of branch target buffer (BTB) entries (col 3 lines 28-38) in parallel with

the branch target buffer (BTB), organizing the recent entry queue as a FIFO queue (col 10 lines 37-40), said Branch Target Buffer (BTB) and said recent entry queue being set associative and said recent entry queue being logically defined as a subset of the Branch Target Buffer (BTB) and coupled to track the last number of branches entered into said BTB (col 10 lines 37-40) and also the most recent entries thereby allowing a comparison of recent entries of said recent entry queue to said BTB (col 10 lines 37-40).

6. Stiles fails to disclose delaying the pipeline until a branch prediction unit finishes the prediction.

Cummins discloses what styles lacks (col 8 lines 32-42)

Stiles would have been motivated to emulate Fig. 7 of Cummins to reduce hardware, processor area, and complexity of correcting the delay.

It would have been obvious at the time of the intention for one of ordinary skill in the art to take the processing system of Stiles and to delay the processor until the branch prediction is completed, as in Cummins.

7. Stiles fails to disclose it comprising blocking an entry matching an entry within the recent entry queue from being written into the BTB and that the BTB and recent entry queue are set associative.

Official Notice is taken that arranging the caches in a tiered arrangement (like a typical L1-L2 cache setup) is well known in the art. A tiered arrangement of cache levels allows the system to write an entry into only the L1 cache rather than spending the time and resources to write into both the L1 and L2. Upon eviction from the L1 cache, the entry is written into the L2. The examiner asserts that with this arrangement,

any entry (including those that match current entries in the L1) will be blocked from writing to the L2 cache.

Official Notice is taken that the recent entry queue (and therefore, BTB) can use set associative rather than direct mapped. Stiles would have been motivated to utilize this change if he desired to alter the size of the recent entry queue. Then a set associative technique would be the preferred technique.

It would have been obvious to one of ordinary skill in the art at the time of invention to have arranged Stiles' caches in a tiered L1-L2 arrangement for the benefit of conserving system resources on writing an entry to the BTB. It further would have been obvious to allow

8. As per claim 4, Stiles teaches the method of claim 3 wherein the recent entry queue is full[y] associative for reading. (Col. 3 lines 63-64)

9. As per claim 8, Stiles teaches the method of claim 1 comprising searching the BTB for a next predicted branch and evaluating the recent entry queue while the BTB is being indexed. (Col. 9 lines 35-37)

10. As per claim 9, Stiles teaches the method of claim 8 wherein the recent entry queue maintains a depth up to the associatively of the BTB whereby while the BTB is indexed, the recent entry queue positions are input to comparison logic. *The examiner asserts that the L1 BPC maintains a depth of as many entries as possible, as dictated by the LRU replacement algorithm (col. 10 lines 37-40). Further, since the L2 BPC is*

disclosed as being direct mapped, (col. 16 line 7) it has an associatively of 1. The L1 BPC has been disclosed as having a depth greater than 1.

11. As per claim 10, Stiles teaches the method of claim 8 comprising searching the recent entry queue [for] a matching branch in parallel to searching BTB output. (Col. 9 lines 35-37)

12. As per claim 11, Stiles teaches the method of claim 10 comprising creating hit detect logic to support the associatively of the BTB. (Col. 16 lines 10-20)

13. As per claim 12, Stiles teaches the method of claim 8 comprising using a subset of the recent entry queue as a subset of the BTB. *The examiner asserts that since an branch data entry can be indexed into both the L1 and L2 BPC, the entries in the L1 BPC constitute a subset of those in the L2.*

14. As per claim 13, Stiles teaches the method of claim 12 comprising fast indexing recently encountered branches. *The examiner asserts that since the L1 BPC holds fewer entries, it inherently can be checked for a pending branch more quickly than the L2 BPC, which stores many more entries.*

15. As per claim 19, Stiles teaches the method of claim 18 comprising delaying decode until a fixed number of cycles. *The decode is inherently delayed by the number of clock cycles it takes to flush the pipeline.*

16. As per claim 20, Stiles teaches the method of claim 19 comprising delaying decode until the BTB predicts a branch. *Inherently, the branch target instruction will not be decoded until it has been predicted to have been taken.*

17. As per claim 21, Stiles teaches the method of claim 1 comprising staging writes to the BTB in the recent entry queue. *The examiner asserts that BTB writes are stored in the L1 BPC (Col. 3 lines 27-38)*

18. As per claim 22, Stiles teaches the method of claim 21 [comprising] delaying a write and placing the write in the recent event queue. *The examiner asserts that a write to the BTB is delayed until the first iteration of the branch has been evaluated for target address and direction. Since the L1 BPC stores this information (col. 3 lines 48-55) it is not possible to place the data in the BPC until it has been calculated.*

19. As per claim 23, Stiles teaches the method of claim 22 [comprising] detecting a predicted branch while its BTB write is temporarily staged in the recent entry queue. (Col. 3 lines 28-38)

20. Claim 24 is directed toward a computer implementing the method of claim 1 and is rejected under the same grounds as stated above.

2. As per claim 27, Stiles teaches the method of claim 2 comprising organizing the recent entry queue as a FIFO queue. (Col. 10 lines 37-40) *The examiner asserts that Stiles' invention removes entries from the L1 BPC in the order in which they were accessed. The first to be accessed are the first to be removed.*

21. Claim 27 is directed toward a computer implementing the method of claim 4 and is rejected under the same grounds as stated above.

22. Claims 28, 31, 34, 38-40, and 46-50 are directed toward a program product implementing the method of claims 1, 4 9-13, and 19-23, respectively, and are rejected under the same grounds as stated above.

23. Claims 14 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles.

24. As per claim 14, Stiles teaches the method of claim 12 but fails to teach it [comprising] searching the complete recent entry queue to block duplicate BTB writes.
25. Official Notice is taken that updating an existing entry in a cache is well known in the art. Checking for an existing entry eliminates the wasting of memory space for a pending store which matches an entry already in the cache.

26. It would have been obvious to one of ordinary skill in the art at the time of invention to have checked the L1 BPC for an existing entry before writing into a new position for the benefit of not wasting memory space.

27. Claim 41 is directed toward a program product implementing the method of claim 14 and is rejected under the same grounds as stated above.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183